

N-Channel MOSFET

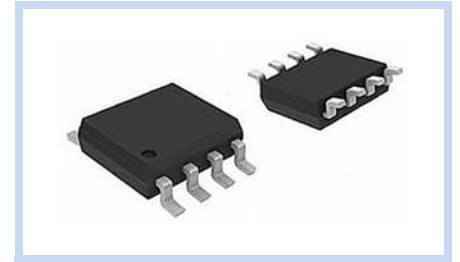
100V 7.0A 2.5W SOP-8

MFT10N7A0S8S

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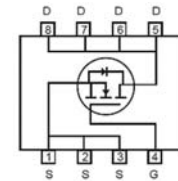
FEATURE

- $R_{DS(ON)} < 25m\Omega$, $V_{GS}=10V$, $I_D=7.0A$
- $R_{DS(ON)} < 28.5m\Omega$, $V_{GS}=4.5V$, $I_D=5.0A$
- High Density Cell Design for Ultra Low On-Resistance
- Advanced Trench Process Technology



MECHANICAL DATA

- Case: SOP-8 package
- Terminal: Solderable per MIL-STD-750, Method 2026

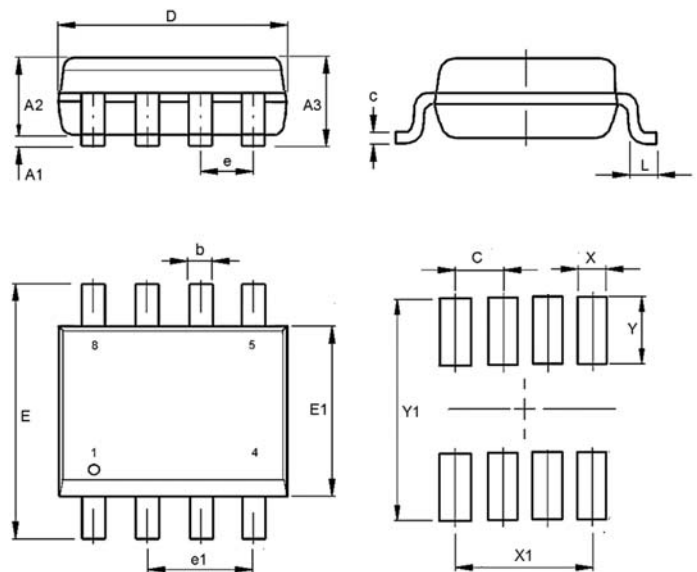


MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current – Continuous	I_D	$T_C=25^\circ C$	7.0
		$T_C=70^\circ C$	5.6
Drain Current – Pulsed	I_{DM}	28	A
Power Dissipation	P_D	$T_C=25^\circ C$	2.5
		$T_C=70^\circ C$	1.6
Single Pulse Avalanche Energy	E_{AS}	8.5	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ C$
Thermal Resistance Junction to Ambient, $t \leq 10s$	$R_{\theta JA}$	50	$^\circ C/W$

DIMENSIONS

Item	Min (mm)	Max (mm)
A1	0.10	0.25
A2	1.35	1.75
A3	1.45	2.00
b	0.31	0.51
c	0.17	0.25
D	4.69	5.00
e	1.27 BSC	
e1	2.54	2.54
E	5.80	6.20
E1	3.70	4.06
L	0.40	0.95
Y	1.00	1.00
Y1	6.75	6.75
X	0.50	0.50
X1	3.81	3.81
C	1.27	1.27



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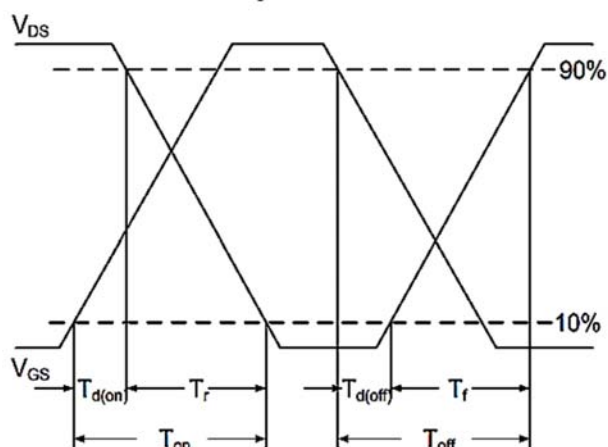
ELECTRICAL CHARACTERISTICS

Off Characteristics	Conditions	Symbol	Min	Typ.	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	BV_{DSS}	100	--	--	V
Zero Gate Voltage Drain Current	$V_{DS}=20V, V_{GS}=0V$	I_{DSS}	--	--	1.0	μA
Gate-Source Leakage Current	$V_{DS}=0V, V_{GS}=\pm 8V$	I_{GSS}	--	--	± 100	μA
On Characteristics	Conditions	Symbol	Min	Typ.	Max	Unit
Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	$V_{GS(th)}$	1.0	1.8	2.5	V
Drain-Source On-Resistance	$V_{GS}=10V, I_D=7.0A$	$R_{DS(on)}$	--	20	25	m Ω
	$V_{GS}=4.5V, I_D=5.0A$		--	22	28.5	
Dynamic Characteristics	Conditions	Symbol	Min	Typ.	Max	Unit
Input Capacitance	$V_{DS}=30V, V_{GS}=0V, F=1.0MHz$	C_{iss}	--	1519	--	pF
Output Capacitance		C_{oss}	--	132	--	pF
Reverse Transfer Capacitance		C_{rss}	--	66	--	pF
Total Gate Charge	$V_{DS}=50V, V_{GS}=10V, I_D=7.0A$	Q_g	--	31	--	nC
Gate-Source Charge		Q_{gs}	--	5.1	--	
Gate-Drain Charge		Q_{gd}	--	7.3	--	
Turn-On Delay Time	$V_{DD}=50V, V_{GS}=10V, R_G=3\Omega, I_D=7.0A$	$T_{d(on)}$	--	11	--	ns
Turn-On Rise Time		T_r	--	42	--	
Turn-Off Delay Time		$T_{d(off)}$	--	40	--	
Turn-Off Fall Time		T_f	--	19	--	
Drain-Source Body Diode	Conditions	Symbol	Min	Typ.	Max	Unit
Drain-Source Diode Forward Current	--	I_S	--	--	7.0	A
Drain-Source Diode Forward Voltage	$V_{GS}=0V, I_S=1.0A$	V_{SD}	--	0.7	1.2	V

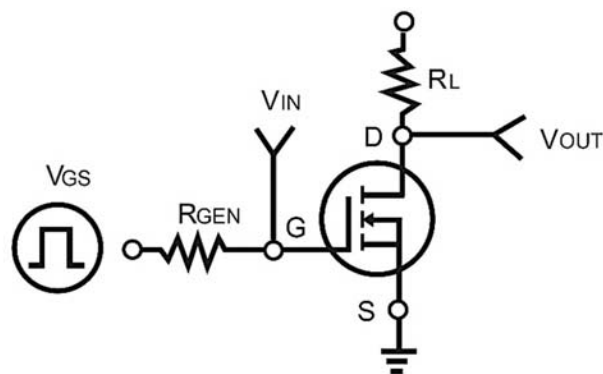
Note:

1. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics
3. The maximum current rating is package limited.
4. Repetitive rating, pulse width limited by junction temperature $T_J(MAX)=150^\circ C$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ C$.
5. The test condition is $L=0.1mH, I_{AS}=13A, V_{DD}=50V, V_{GS}=10V$
6. $R_{\theta JA}$ is the sum of the junction to case to ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1inch FR-4 with 2oz. square pad of copper.
7. Guaranteed by design, not subject to production testing.

Switching Time Waveform



Switching Test Circuit



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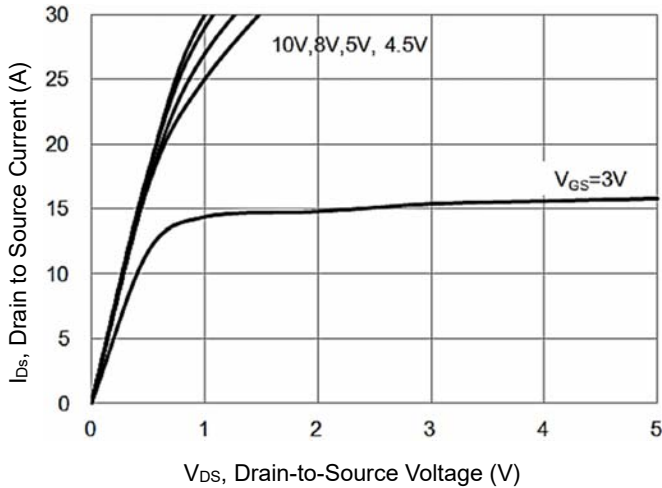
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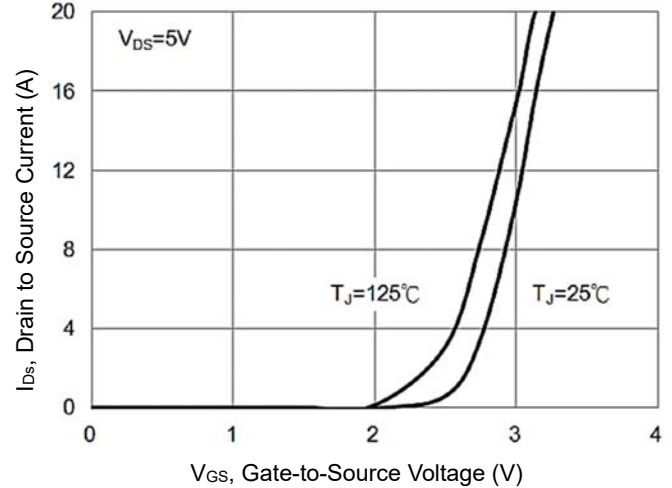
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CHARACTERISTIC CURVES

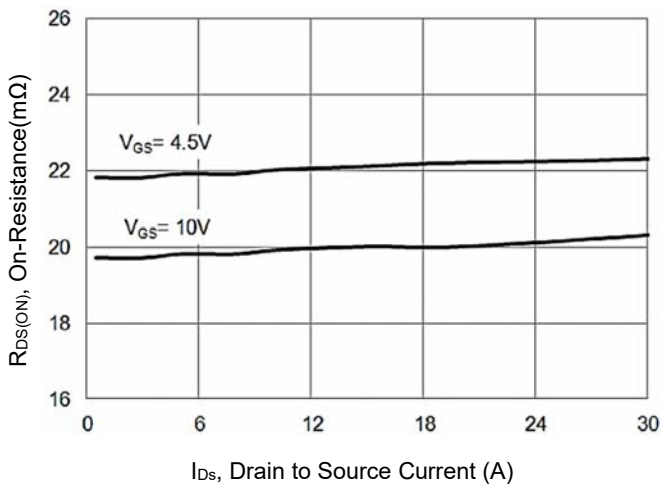
On-Region Characteristics



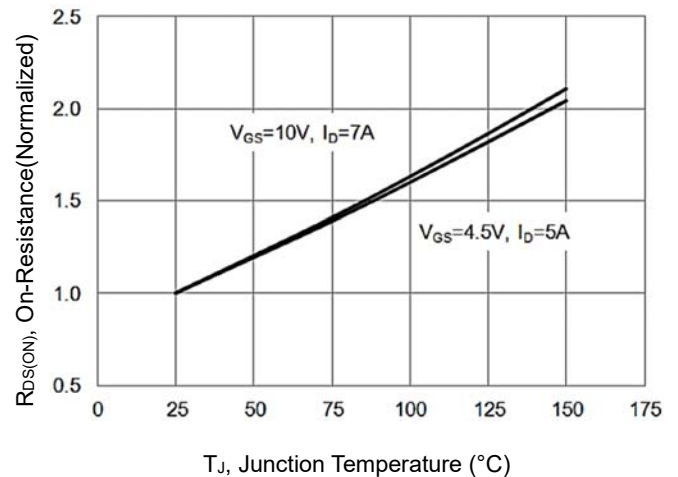
Transfer Characteristics



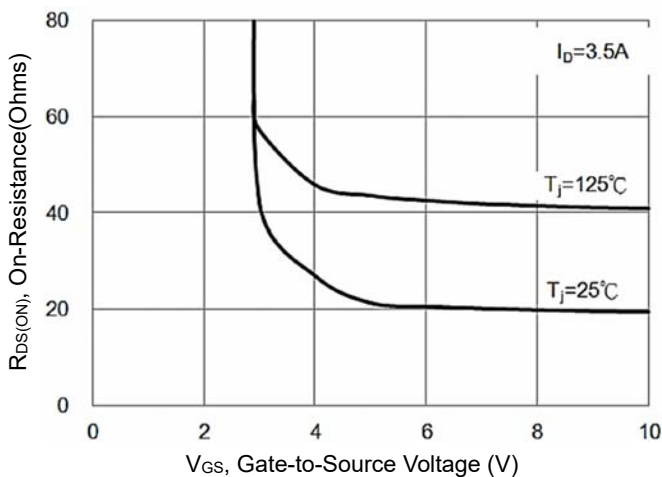
On-Resistance Variation vs. Drain Current



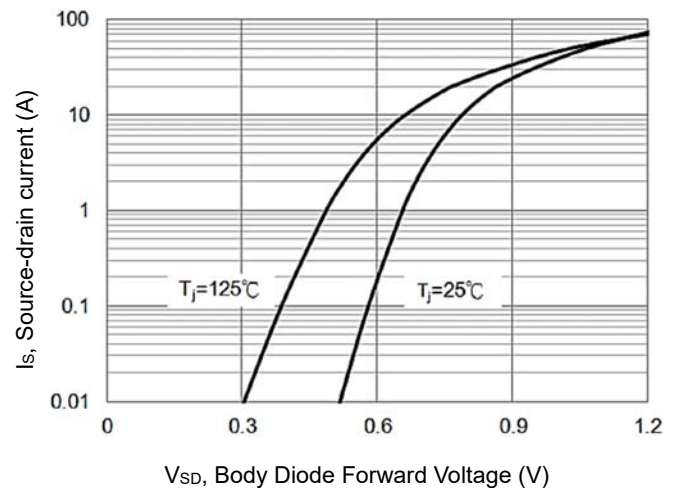
On-Resistance Variation vs. Temperature



On-Resistance Variation vs. Vgs



Body Diode Characteristics



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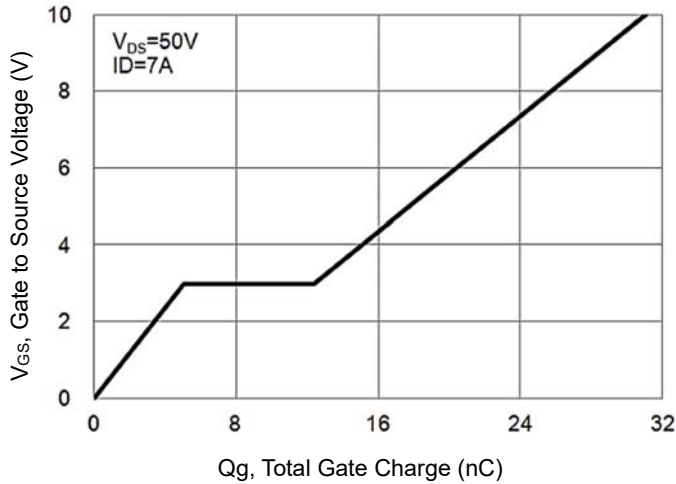
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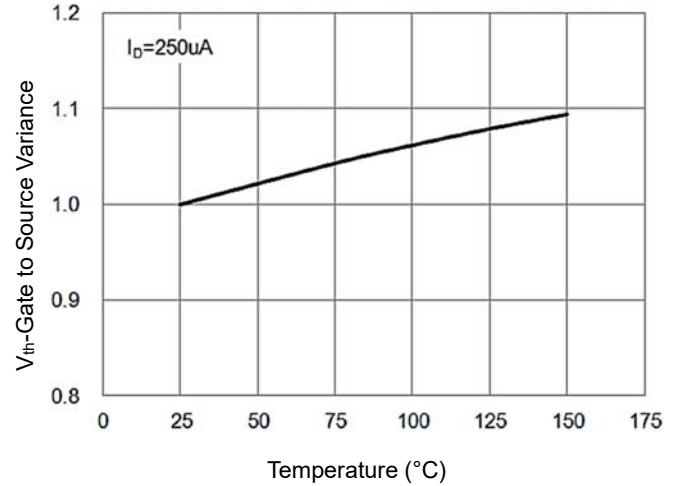
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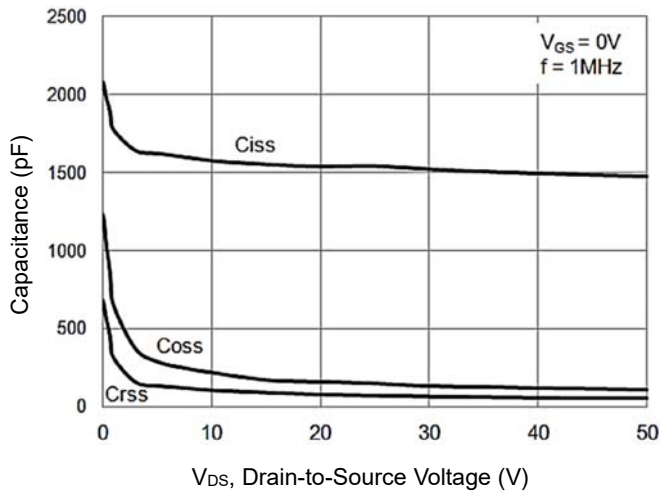
Gate Charge Characteristics



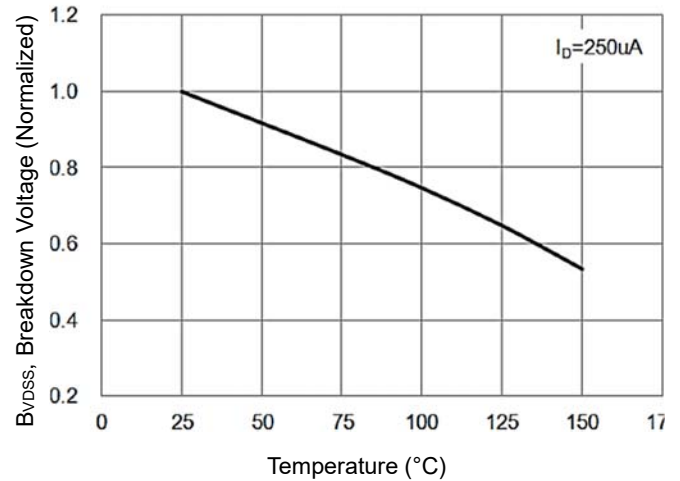
Threshold Voltage Variation with Temperature



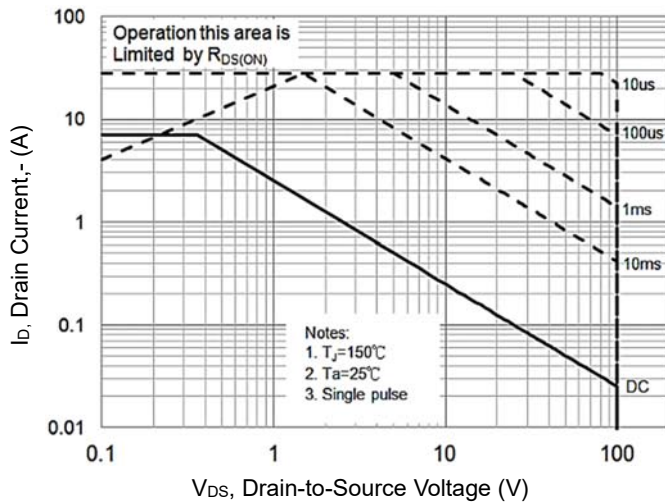
Capacitance vs. Drain Source Voltage



Breakdown Voltage Variation vs. Temperature



Maximum Safe Operating Area

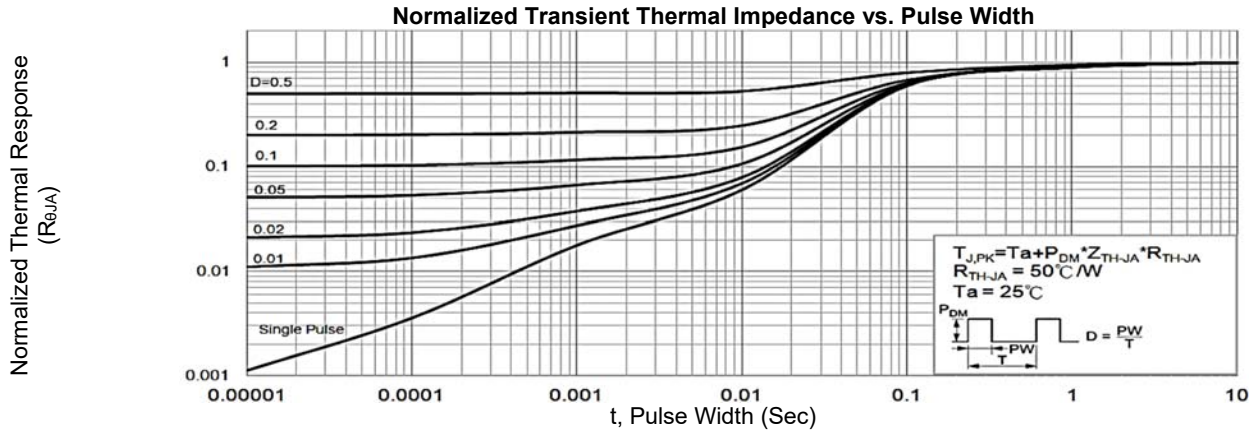


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CHARACTERISTICS CURVES



MARKING LAYOUT



L9458AL Marking code
 Y Last digit of calender
 W Week Code
 LLX Wafer Lot#, Line#