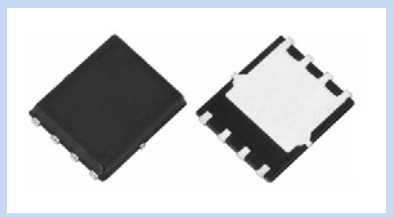
N Channel MOSFET
100V 35A 62W DFN3×3

MFT10N35D33

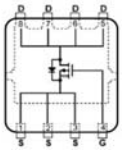
MERITEK

FEATURE



- $R_{DS(ON)}$<25mΩ, V_{GS}=10V, I_D=15A
- $R_{DS(ON)}$<28.5mΩ, V_{GS}=4.5V, I_D=10A
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High Switch Speed
- Low reverse transfer capacitance

MECHANICAL DATA



RoHS

- Case: DFN3×3-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026

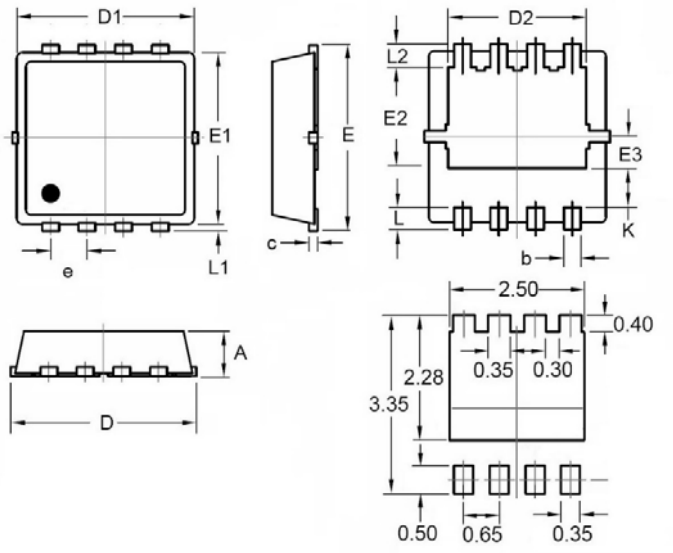
MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current – Continuous	T_C=25°C	I_D	35	A
	T_C=100°C		22	
Drain Current – Pulsed	T_C=25°C	I_{DM}	140	A
Power Dissipation	T_C=25°C	P_D	62	W
	T_C=100°C		25	
Drain Current – Continuous	T_A=25°C	I_D	6.3	A
	T_A=70°C		5	
Power Dissipation	T_A=25°C	P_D	2.0	W
	T_A=70°C		1.3	
Single Pulse Avalanche Energy		E_{AS}	54	mJ
Thermal Resistance Junction to Case		$R_{\theta JC}$	2	°C/W
Thermal Resistance Junction to Ambient		$R_{\theta JA}$	62.5	°C/W
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to +150	°C

Note:
1. The test condition is L=3mH, I_{AS}=6A, V_{DD}=50V, V_{GS}=10V,Starting T_J=25°C

DIMENSIONS

Item	Min. (mm)	Max. (mm)
A	0.70	0.85
b	0.20	0.40
c	0.10	0.25
D	3.15	3.45
D1	3.00	3.25
D2	2.29	2.65
E	3.15	3.45
E1	2.90	3.20
E2	1.54	1.94
E3	0.37	0.77
e	0.65(BSC)	
K	0.50	0.89
L	0.30	0.50
L1	0.06	0.20
L2	0.27	0.57

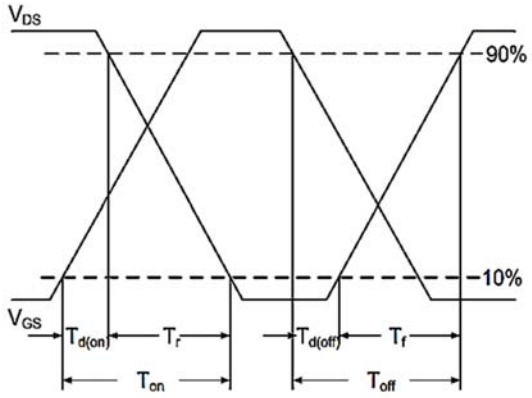


ELECTRICAL CHARACTERISTICS

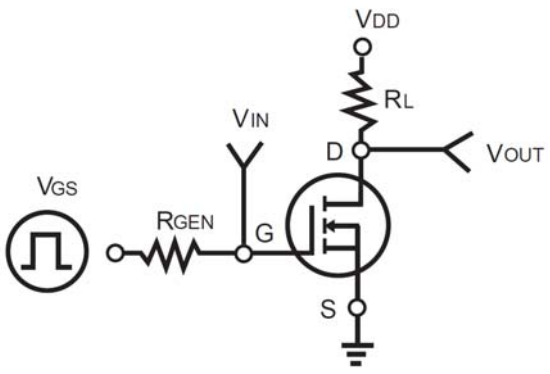
Off Characteristics	Conditions	Symbol	Min	Typ.	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250μA	BV_{DSS}	100	--	--	V
Drain-Source Leakage Current	V_{DS}=80V, V_{GS}=0V,	I_{DSS}	--	--	1	μA
Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0V	I_{GSS}	--	--	±100	nA
On Characteristics	**Conditions**	**Symbol**	**Min**	**Typ.**	**Max**	**Unit**
Static Drain-Source On-Resistance	V_{GS}=10V, I_D=15A	$R_{DS(ON)}$	--	20	25	mΩ
	V_{GS}=4.5V, I_D=10A		--	22	28.5	
Gate Threshold Voltage	V_{GS}=V_{DS} , I_D=250μA	$V_{GS(th)}$	1	1.73	2.5	V
Dynamic Characteristics	**Conditions**	**Symbol**	**Min**	**Typ.**	**Max**	**Unit**
Total Gate Charge	V_{DS}=50V, V_{GS}=10V, I_D=10A	Q_g	--	31	--	nC
Gate-Source Charge		Q_{gs}	--	5.1	--	
Gate-Drain Charge		Q_{gd}	--	7.3	--	
Turn-On Delay Time	V_{DS}=50V, V_{GS}=10V, R_G=3Ω, I_D=10A	$T_{d(on)}$	--	11	--	nS
Rise Time		T_r	--	42	--	
Turn-Off Delay Time		$T_{d(off)}$	--	40	--	
Fall Time		T_f	--	19	--	
Input Capacitance	V_{DS}=30V , V_{GS}=0V , F=1MHz	C_{iss}	--	1519	--	pF
Output Capacitance		C_{oss}	--	132	--	
Reverse Transfer Capacitance		C_{rss}	--	66	--	
Drain-Source Body Diode	**Conditions**	**Symbol**	**Min**	**Typ.**	**Max**	**Unit**
Diode Forward Current	--	I_S	--	--	35	A
Diode Forward Voltage	V_{GS}=0V , I_S=1A	V_{SD}	--	0.68	1.2	V

Note:
2. Pulse width≤300μs, duty cycle≤2%
3. Guaranteed by design,not subject to production testing
4. The maximum current rating is package limited
5. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.
6. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a I inch^2 with 2oz square pad of copper.
7. Essentially independent of operating temperature typical characteristics.

Switching Time Waveform

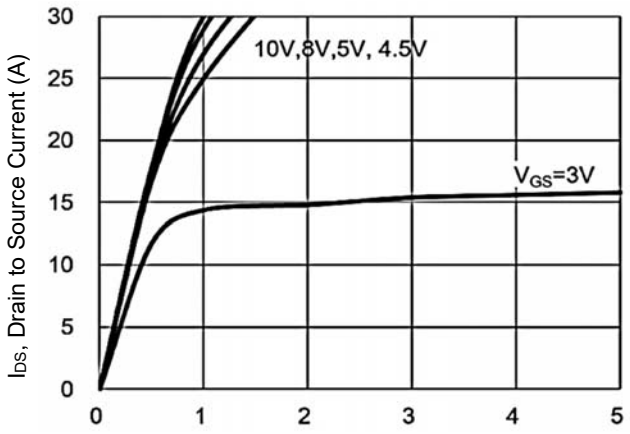


Switching Test Circuit



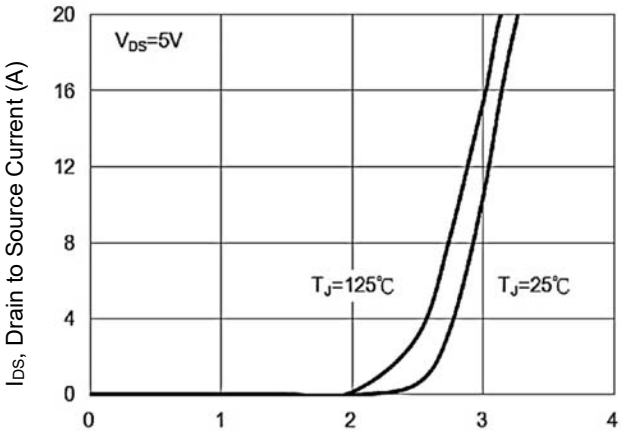
CHARACTERISTIC CURVES

On-Region Characteristics



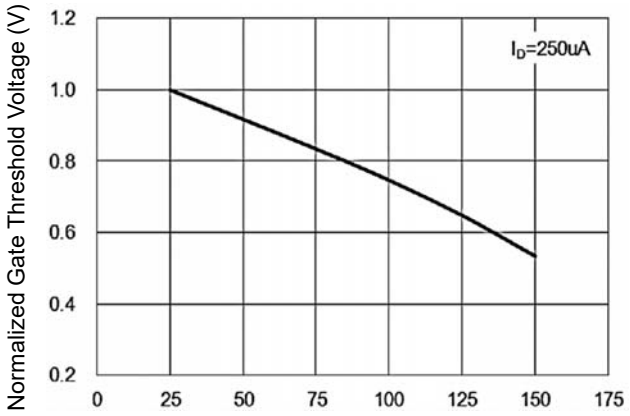
V_{DS}, Drain to Source Voltage (V)

Transfer Characteristics



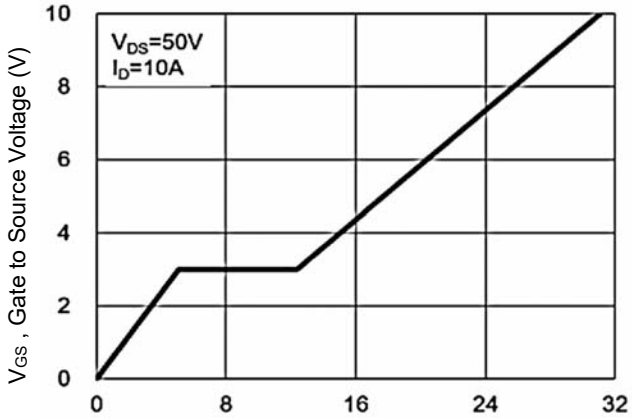
V_{GS}, Gate to Source Voltage (V)

Normalized V_{th} vs. T_J



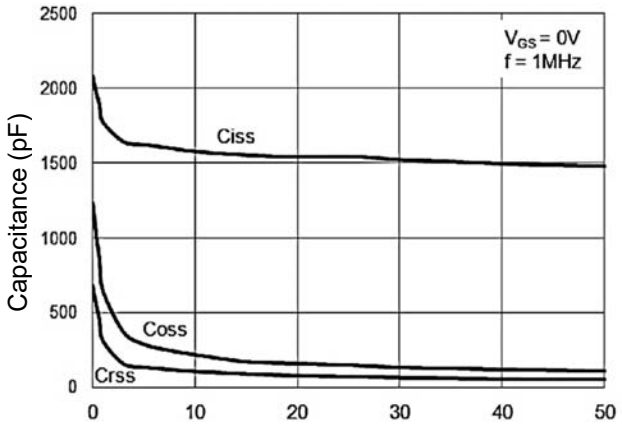
T_J , Junction Temperature (°C)

Gate Charge Waveform



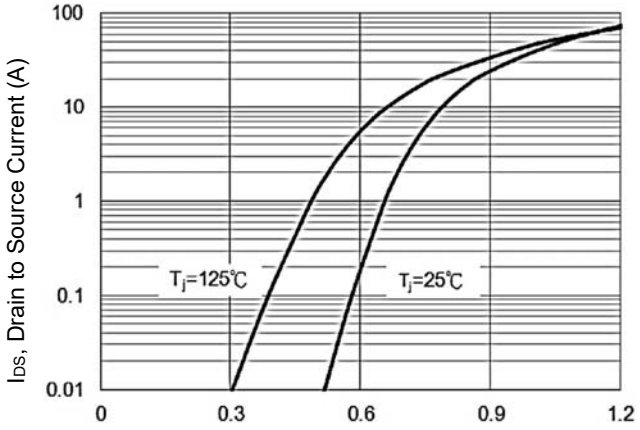
Qg , Gate Charge (nC)

Capacitance vs. Drain-Source Voltage



V_{DS}, Drain-to-Source Voltage (V)

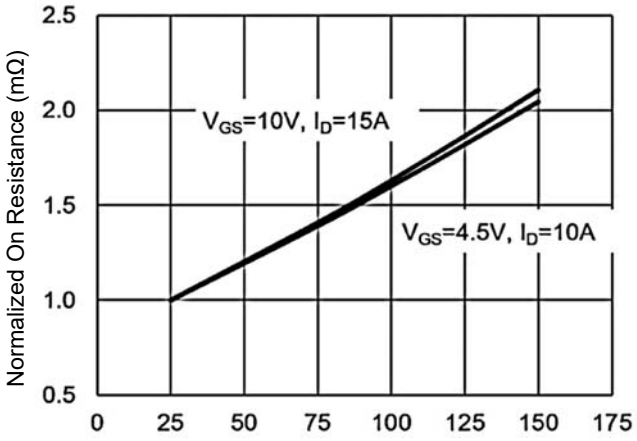
Body Diode Forward Voltage



V_{SD}, Source to Drain Voltage (V)

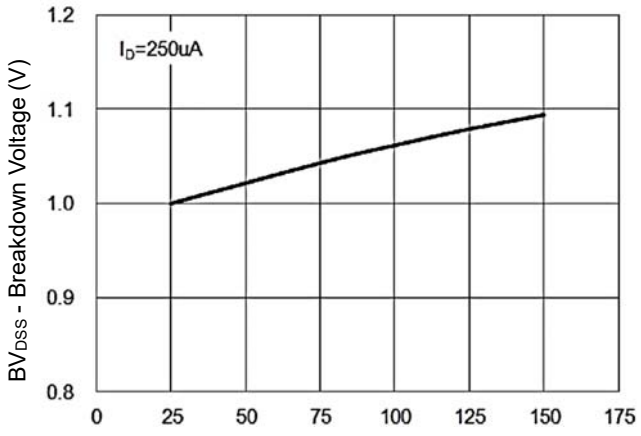
CHARACTERISTIC CURVES

On-Resistance vs Junction Temperature



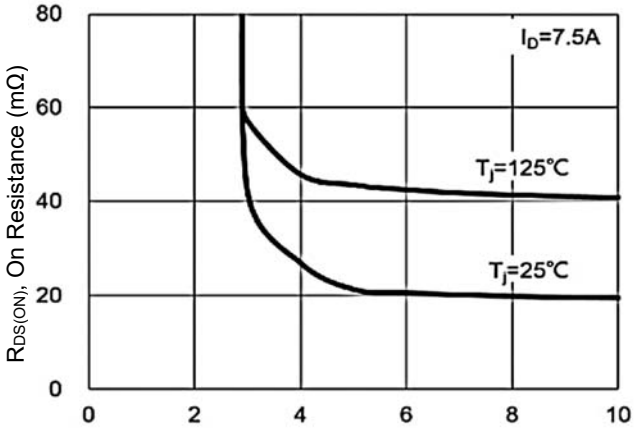
T_J , Junction Temperature (°C)

Breakdown Voltage vs Temperature



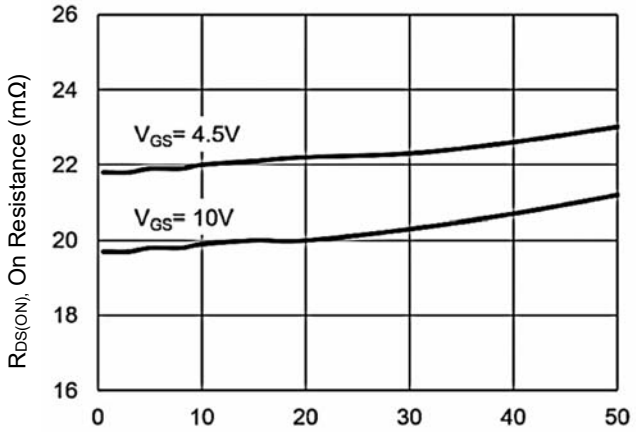
T_J , Junction Temperature (°C)

On-Resistance Variation with V_{GS}



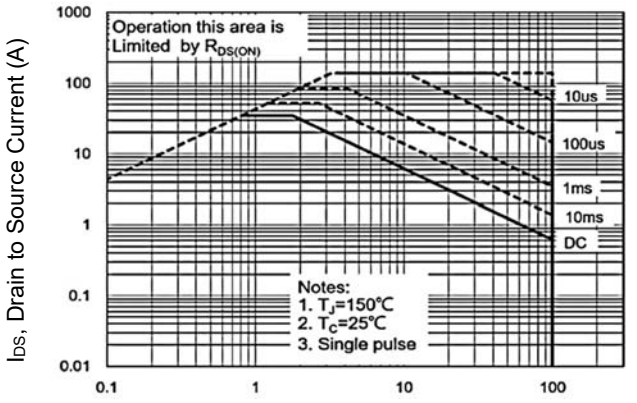
V_{GS}, Gate to Source Voltage (V)

On-Resistance vs. Drain Current



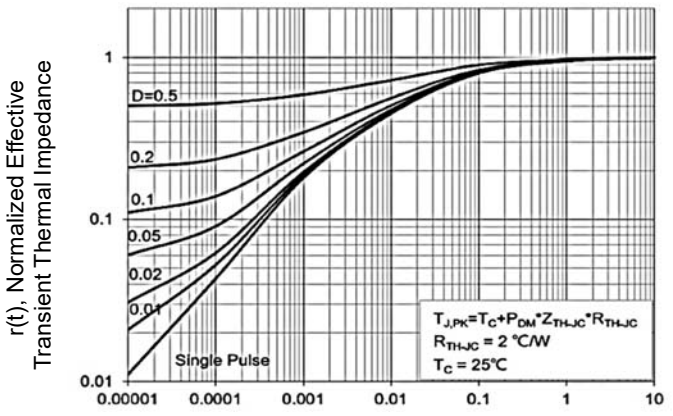
I_{DS}, Drain to Source Current (A)

Maximum Safe Operating Area



V_{DS}, Drain-to-Source Voltage (V)

Normalized Transient Thermal Impedance Curves



Square Wave Pulse Duration (s)